REMARKS

Claims 3, 5-11, 14, 16-22, 25, and 27-33 are pending in the application. The Examiner's reconsideration of the rejections in view of the remarks is respectfully requested.

Applicants appreciate the withdrawal of the rejection under 35 USC 101.

Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33 have been rejected under 35 USC 103(a) as being unpatentable over Fossum et al. (USPN 4,888,679) in view of Birrittella (USPN 6,266,759). The Examiner stated essentially that the combined teachings of Fossum and Birrittella teach or suggest all of the limitations of Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33.

Claims 3, 9, 10, 11, 14, 25, and 31-33 are the independent claims.

Claims 3, 9, 10, and 11 recite, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array." Claims 14, 25 and 31 claim, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file." Claim 32 claims, *inter alia*, "providing a

pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries having arbitrary starting addresses are grouped into addressable words corresponding to individual data vectors stored in the vector data file." Claims 33 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file; wherein, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array."

By the Final Office Action, the Examiner suggested essentially that Fossum teaches a tag A address corresponding to data word entries grouped by the address decoder corresponding to the vectors. Applicants respectfully disagree; the tags are associated with the blocks (see col. 6, lines 35-40) and the blocks store vectors which extend across one or more blocks (see col. 6, lines 10-11). However, there is no teaching or suggestion that the tags are "grouped into addressable words corresponding to individual data vectors" as claimed. Indeed, the tag store merely includes slots storing individual addresses (see FIG. 2 and 48-52). The tag store clear is not arranged to store addressable words, essentially as claimed. That is, multiple tags do not have

a shared word address ("grouped into addressable words"). Therefore, Fossum fails to teach all the limitations of Claims 3, 9, 10, 11, 14, 25, and 31-33.

Birrittella fails to cure the deficiencies of Fossum described above; Birrittella does not teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14, 25, and 31, and essentially as claimed in Claims 32-33. Birrittella teaches that a vector address is addressed by a first element of the vector and additional elements are stored at fixed intervals (see col. 4, lines 60-65) Birrittella method for addressing the vector is not analogous to an addressable word corresponding to a vector, essentially as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33. For example, see FIG. 2, which illustrates a memory-reference vector instruction. The memory-reference vector instruction includes only a single address of a register and further includes a vector length, implying a contiguous vector. Birrittella fails to teach or suggest an addressable word, essentially as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33. Therefore, Birrittella fails to cure the deficiencies of Fossum.

The Examiner further suggested that while Fossum did not specifically show the arbitrary starting address as claimed, Birrittella taught an arbitrary starting address. A careful search of Birrittella reveals only arbitrary offsets from a base address of a vector (see col. 3, line 16 and col. 4, line 65). Birrittella simply does not teach or suggest an arbitrary base address ("arbitrary starting address" as claimed). Further, with respect to Claim 32, the combined teachings of Fossum and Birrittella fail to teach or suggest "entries having arbitrary starting addresses are grouped into addressable words" (see for example, FIG. 4 of the application. Neither Fossum or Birrittella teach a vector having non-contiguous data elements.

The combined teachings of Fossum and Birrittella teach a method for calculating

addresses of vector memory-reference instructions. The combined teachings of Fossum and Birrittella fails to teach or suggest "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14, 25, and 31-33.

Claims 7, 16-18, 29, and 30 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 7, 16-18, 29, and 30.

Claim 7 depends from Claim 3. Claims 16-18 depend from Claim 14. Claims 29 and 30 depend from Claim 25. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

Claims 5, 6, 27, and 28 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 5, 6, 27, and 28.

Claims 5 and 27 are the independent claims.

Claim 5 claims, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one

storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array." Claim 27 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file."

As presented above, the combined teachings of Fossum and Birrittella fails to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file."

Sakakibara fails to cure the deficiencies in the combined teachings of Fossum and Birrittella in this regard; Sakakibara teaches that a vector register unit 170 holding actual vector elements (see col. 11, lines 33-40). The vector register unit does not store entries or pointers to a vector data file, essentially as claimed. Indeed, nowhere does Sakakibara teach or suggest the use of a pointer array, much less entries identifying at least one storage element in the vector data file. Therefore, Sakakibara fails to cure the deficiencies in the combined teachings of Fossum and Birrittella.

The combined teachings of Fossum, Birrittella and Sakakibara fail to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 5 and 27.

Claims 6 and 28 depend from Claims 5 and 27, respectively. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including Claims 3, 5-11, 14, 16-22 and 25, 27-33, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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